Final Exam
CPSC/ELEN 680
May 5, 2003

Name: ____

5-Digit Student ID: ___________

Instructions

This exam is closed book. Provide brief but complete answers to the following questions in the space provided, using figures as necessary. Show your work for partial credit.

1. For the circuit in Figure 1, do the following:
   i. (5 pts) Count the total number of single stuck-at fault sites.
   ii. (5 pts) Show that the three single faults *H* s-a-1, *J* s-a-1 and *K* s-a-1 are equivalent.
   iii. (5 pts) Using the parallel fault simulation algorithm with a 4-bit machine word, determine which of the three single faults, *F* s-a-1, *H* s-a-0, and *L* s-a-1, are detected by the input vector A=1, B=0. Show the machine word usage. You may draw on the figure as part of your solution.

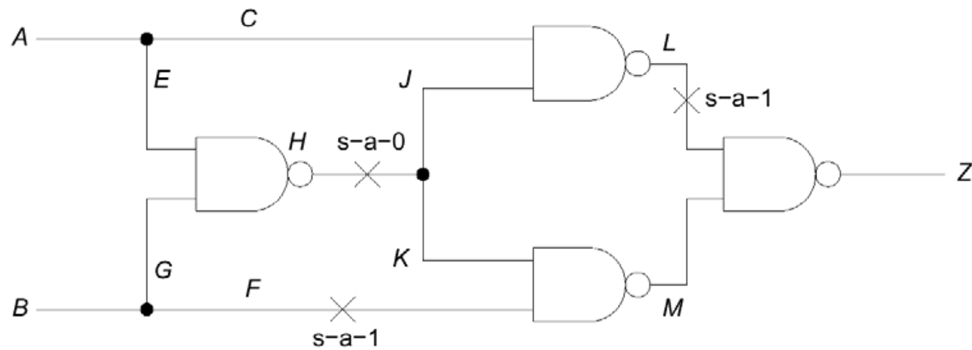

Figure 1. Circuit for Problem 1.

2. Consider the circuit under test (CUT) with two outputs *C* and *S*, shown in Figure 2. We desire a test that will detect a target fault at any one output but not at both outputs. To enforce this in the ATPG, Figure 2 gives an ATPG model circuit in which the two outputs of the CUT are combined into an XOR gate (shown shaded) to produce an output *Z*.
   i. (5 pts) Show that when a fault is detected at *Z* in the ATPG model, it must be exclusively detected either at *C* or at *S*.
   ii. (5 pts) Using either the five-valued or nine-valued logic, obtain a test to detect *B* s-a-1 at one but not both of *C* or *S*.
   iii. (5 pts) Can a test be found for *H* s-a-0 that only propagates to one but not both of *C* or *S*?

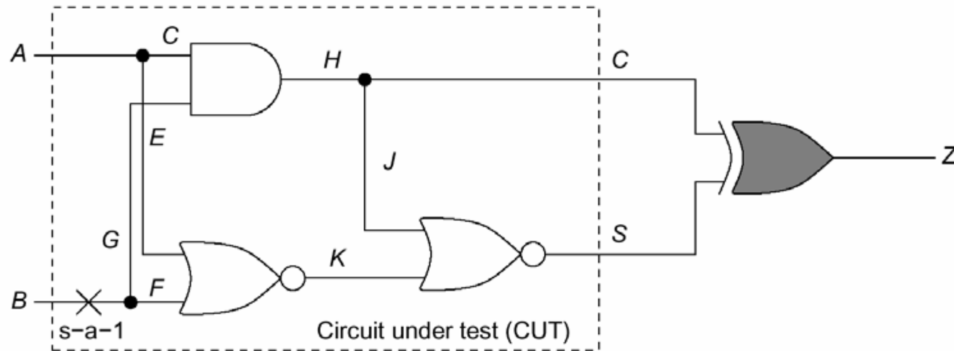

Figure 2. Circuit for Problem 2.

3. (15 pts) For the circuit in Figure 3, compute the combinational and sequential SCOAP testability measures (both controllability and observability, including the *CLOCK* and synchronous *~RESET* signals). You can write on the figure, but be clear about which measure is which. Extra copies of the circuit are attached at the end to aid you in working out your solution.

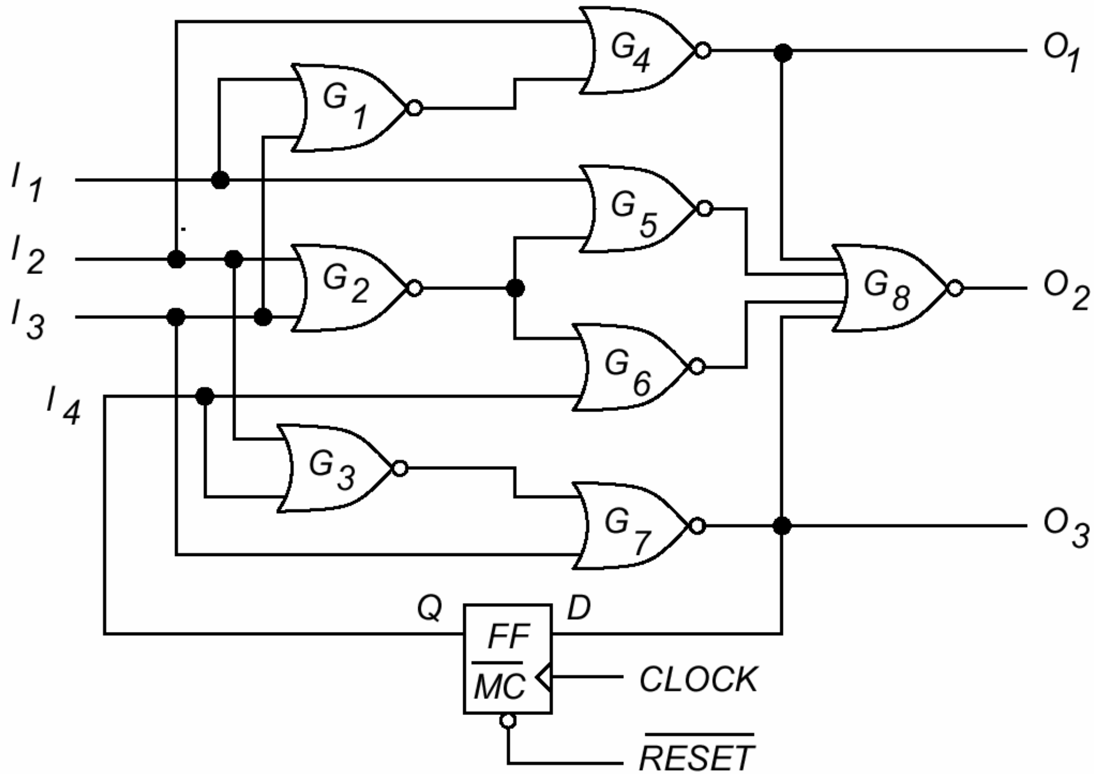

Figure 3. Circuit for Problem 3.

4. i. (5 pts) Specify a single input change (SIC) test for the critical path a to z with a rising transition on a (shown in bold lines) in the circuit of Figure 4(i). Is this a robust test?
ii. (5 pts) The circuit of Figure 4(i) is redesigned in Figure 4(ii) to reduce the delay. Will the SIC test obtained above still test the longest delay path shown in bold lines? If not, what is the minimum modification required in the test?

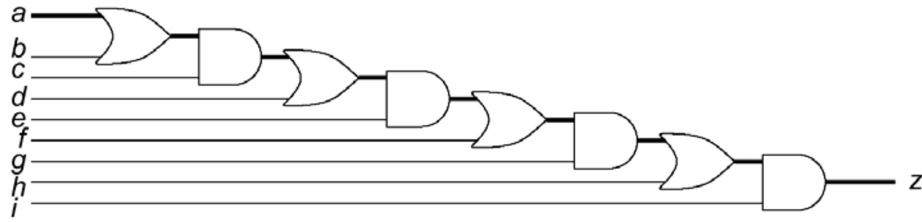

Figure 4(i) Original circuit for Problem 4.

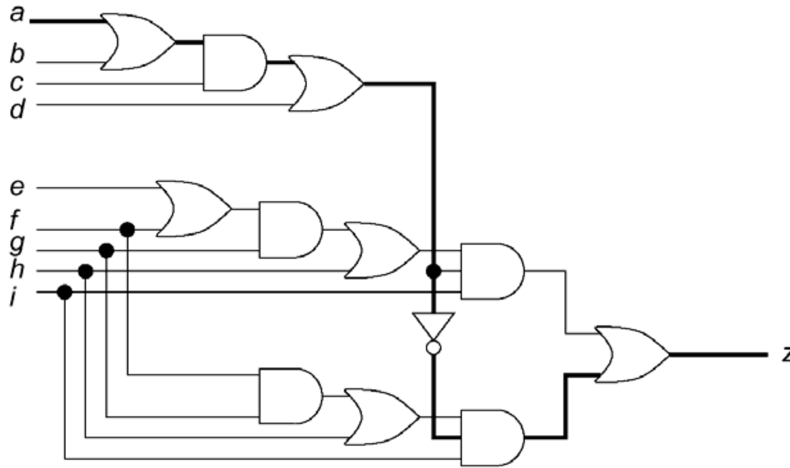

Figure 4(ii). Redesigned circuit for Problem 4.

5. The memory test MARCH C– is $\{\Updownarrow(w0);\ \Uparrow(r0,w1);\Uparrow(r1,w0);\Downarrow(r0,w1);\ \Downarrow(r1,w0);\ \Updownarrow(r0)\}$. The symbol $\Updownarrow$ is meant to be the up/down direction symbol.

   i. (5 pts) What is the testing time complexity of MARCH C– in terms of *n*, the number of bits in the memory?

   ii. (5 pts) Show whether or not this test can detect all transistor stuck-open faults in an SRAM made of the six-transistor cells shown in Figure 5. For reading, the bit lines are first precharged to 1, and then one line discharges to 0 through the *C* or *D* pass transistor. For writing the bit lines are set to the appropriate values and then the *WORD* line is selected.

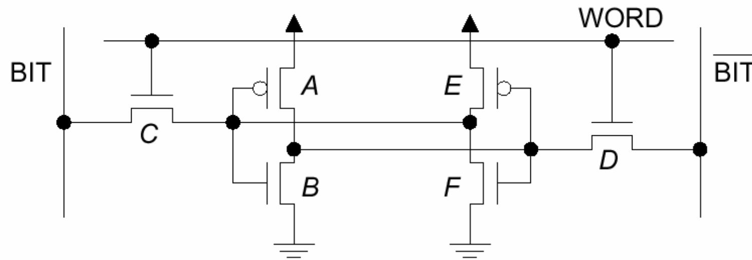

Figure 5. Six-transistor SRAM cell for Problem 5(ii).

6. i. (5 pts) For an analog circuit, the test waveform frequency $F_t = 2010$ Hz and the sampling frequency in the DSP ATE is 8000 s/s. Compute the minimum *unit test period* (UTP) and the corresponding *primitive frequency*.
ii. (5 pts) A circuit is to be tested on a DSP ATE with *sampling rate* $F_s = 8000$ s/s. Originally, the *integration interval* or *test interval* $P = 40$ ms, but that does not allow the number of *sampling intervals* $N \geq 400$. What is a test waveform frequency as close to 2000 Hz as possible that still generates $N \geq 400$ unique samples by adjusting the *primitive frequency* Δ? How many *test waveform cycles* (M) will there be in the *primitive period*?

7. The circuit in Figure 6 is a sequence detector. A sequence 111 in the *INPUT* bit-stream locks the output *Z* to 1. The state of the circuit can be set to 000 with output *Z*=0 by applying *CLEAR*=1.
   i. (5 pts) Redesign the circuit using minimum extra hardware to conform to the scan design rule, "clock must not be gated by a combinational signal." Neatly sketch the redesigned circuit.
   ii. (5 pts) Sketch the schematic of the full-scan circuit using the multiplexer type of scan flip-flops (SFFs). You do not need to show the internals of the multiplexer. Show the complete wiring of the *SCANIN*, *SCANOUT*, and test mode (*TM*) signals.

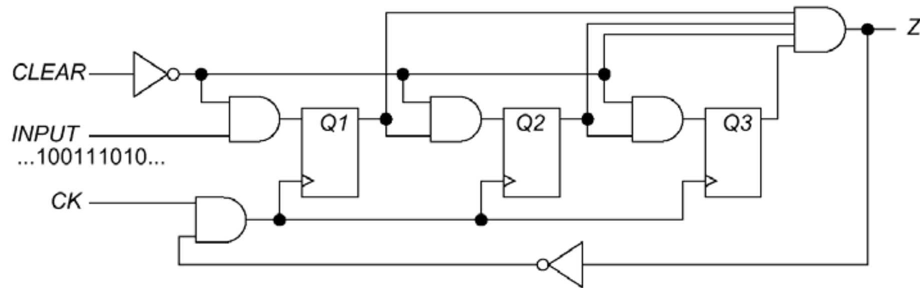

Figure 6. Circuit for Problem 7.

8. i. (5 pts) Draw the schematic for an external-XOR LFSR pattern generator implementing the characteristic polynomial $1+x^2+x^3$. Include initialization of the flip-flops via their set/reset pins.
ii. (5 pts) Assume a circuit tested by an exhaustive counter-based pattern generator and the MISR response compactor shown in Figure 7. (The muxed primary inputs are also shown). The MISR is initialized to 000. What is the good machine result (signature) in the MISR?
iii. (5 pts) What is the bad machine signature for the fault q s-a-0? Does the test hardware alias for this fault?

Figure 7. CUT with counter and MISR for Problem 8.

9. (10 pts extra credit) Figure 8 shows two boundary scan cells surrounding some on-chip system logic. We test the path from the INPUT boundary scan cell, through the on-chip system logic, and ending at the OUTPUT boundary cell. The JTAG (IEEE 1149.1) commands are: SAMPLE, PRELOAD, EXTEST, INTEST, RUNBIST, CLAMP, IDCODE, USERCODE, HIGHZ, and BYPASS. Please explain the sequence of these commands used for delay fault testing of this particular path and the action and purpose of each command used.

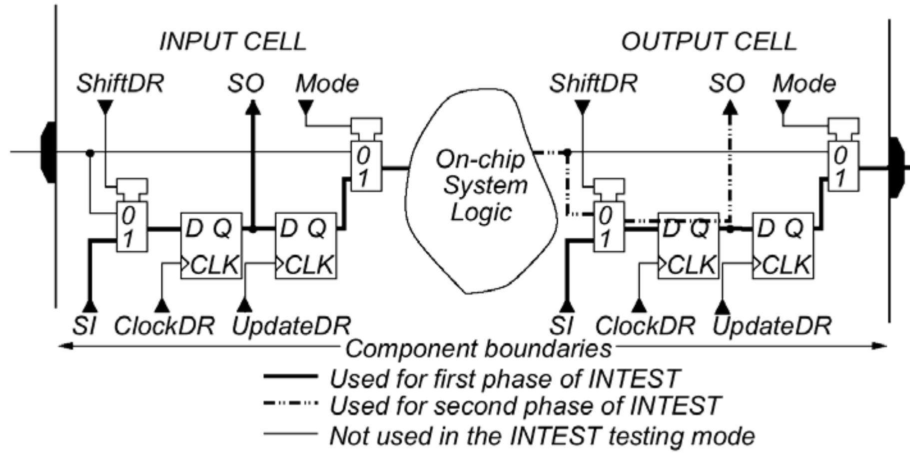

Figure 8. Circuit for Problem 9.

Extra sheet for Problem 3.