

Name: _____

UIN: _____

Instructions

This exam is closed book. Provide brief but complete answers to the following questions in the space provided, using figures as necessary. Show your work for partial credit.

1. For the circuit in Figure 1, do the following:
 - i. (5 pts) Count the total number of path delay faults. For each path list the lines in the path, e.g. A-C-L-Z.
 - ii. (5 pts) Count the total number of transition faults.
 - iii. (5 pts) For each SAF at F, H and L, describe a path delay test (input vector pair and list of lines in the path), if one exists, that will cause a corresponding transition at the fault site. For a SA0, generate a rising transition. For a SA1, generate a falling transition. If a test does not exist, explain why. If the test is robust, explain why it is robust.

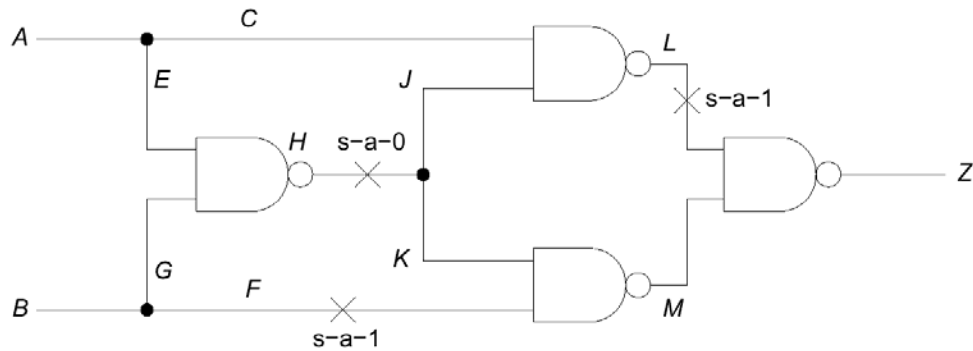


Figure 1. Circuit for Problem 1.

3. (15 pts) For the circuit in Figure 3, compute the combinational and sequential SCOAP testability measures - both controllability and observability, including the *CLOCK*. The flip-flops do not have a reset line. Write your SCOAP measures on the figure using standard notation. Extra copies of the circuit are attached at the end to aid you in working out your solution.

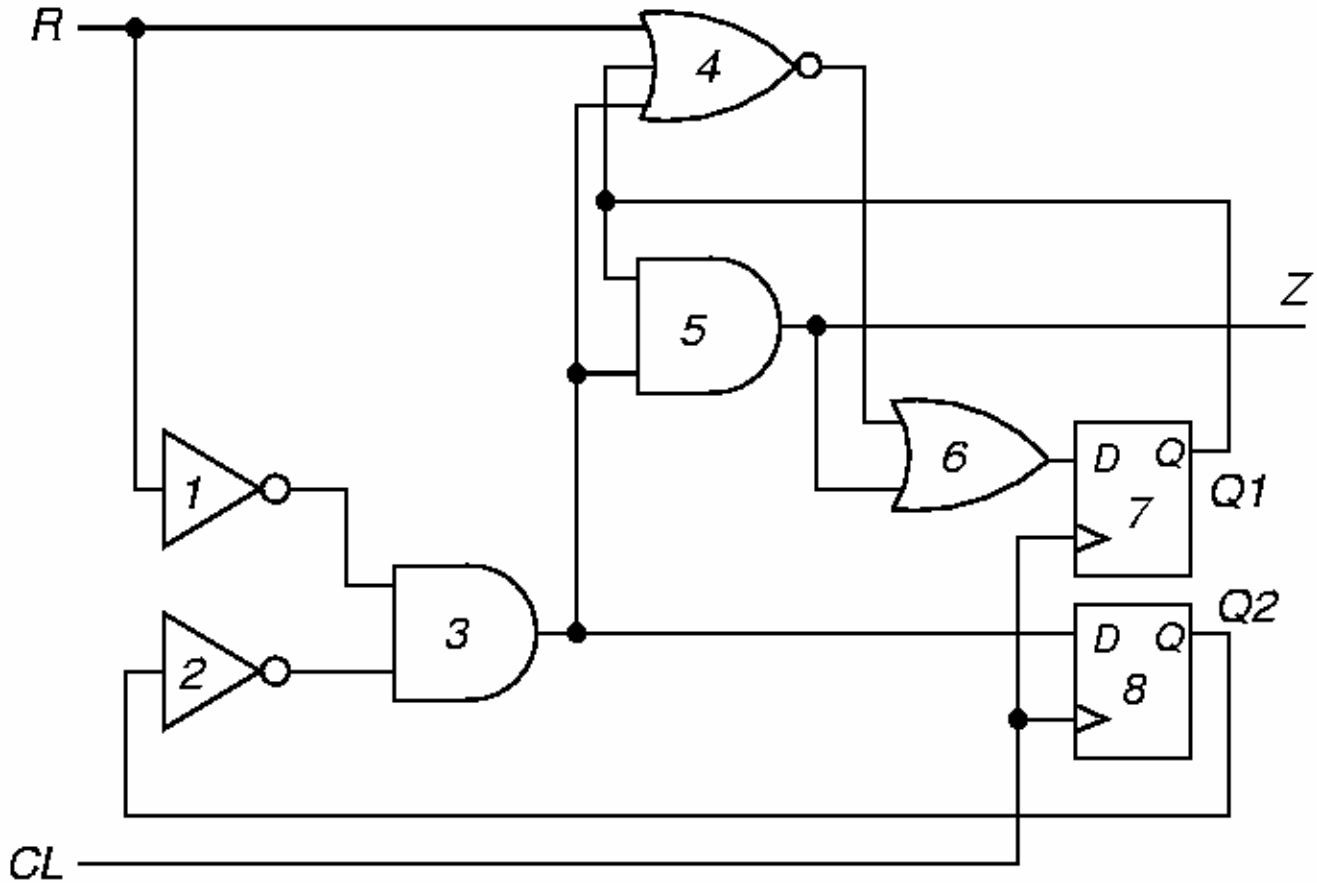


Figure 3. Circuit for Problem 3.

4. A set of patterns in a RAM are shown in Figure 4. Consider the “March A” algorithm that consists of five march elements: M1, M2, M3, M4 and M5, given below, applied in the order M1 M2 M3 M4 M5.

M1: \uparrow (W0) M2: \uparrow (R0, W1, W0, W1) M3: \uparrow (R1, W0, W1) M4: \downarrow (R1, W0, W1, W0) M5: \downarrow (R0, W1, W0)

- i. (8 pts) On each of the patterns in Figure 4, indicate if that pattern is applied during the March A algorithm or not. If the pattern is applied, list all the march elements in which the pattern is applied.
- ii. (4 pts) Consider a fault that causes a base cell to become 1 whenever its four neighbors are all 0s. List all the march elements that will detect such a fault during the March A algorithm.
- iii. (3 pts) Consider a more complex fault that causes the base cell to be 1 whenever its North East West South neighbors are 1000 and the cell becomes a 0 whenever the neighbors are 1100, irrespective of the original value in the base cell. What march elements in March A will detect this fault?

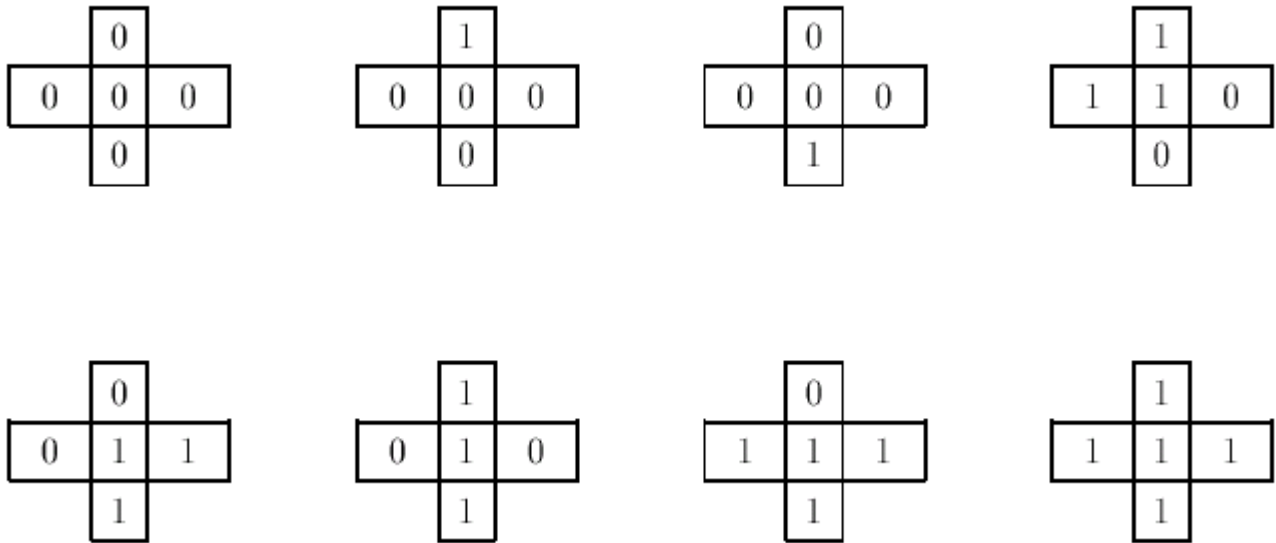


Figure 4. Figure for Problem 4.

5. (15 pts) Using structural fault equivalence, list all the faults in Figure 5 that are equivalent.

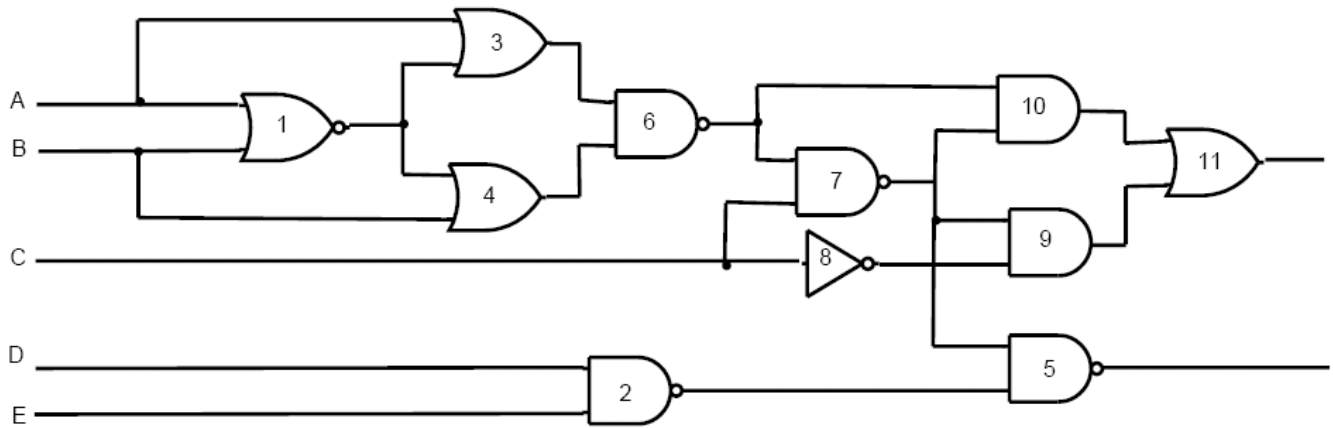


Figure 5. Figure for Problem 5.

6. Consider the yield equation below, where T is the fault coverage, A is the chip area, f is the fault density and β is the fault clustering coefficient.

$$Y(T) = \left(1 + \frac{TAf}{\beta}\right)^{-\beta}$$

- i. (6 pts) Consider a chip with area 0.9 cm^2 with maximum fault coverage of 90%. The fault density is $2.333 \text{ faults/cm}^2$ and $\beta = 0.083$. What is the expected yield of the design? What is the expected defect level (DL)?
- ii. (9 pts) You add DFT to increase the fault coverage to 95%. The DFT increases chip area by 5%. What is the relative improvement in product quality, defined as $(old_DL - new_DL)/old_DL$?

7. i. (5 pts) Draw the schematic for a modular LFSR (XOR gates between the flip-flops) implementing the characteristic polynomial $1+x+x^3+x^5$. Include initialization of the flip-flops via their set/reset pins.
- ii. (5 pts) Assume a circuit in Figure 7 tested by the shifting sequence for inputs ABC: 000, 001, 011, 111, 110, 100. The output feeds the MISR shown. The MISR is initialized to 000. What is the good machine result (signature) in the MISR?
- iii. (5 pts) What is the bad machine signature for the fault q s-a-0? Does the test hardware alias for this fault?

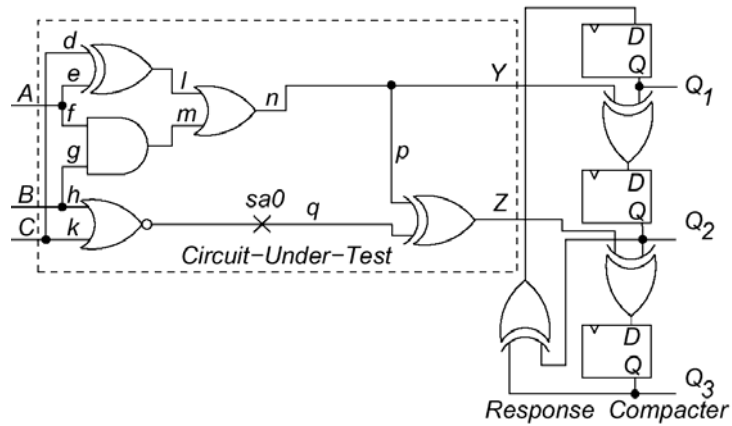
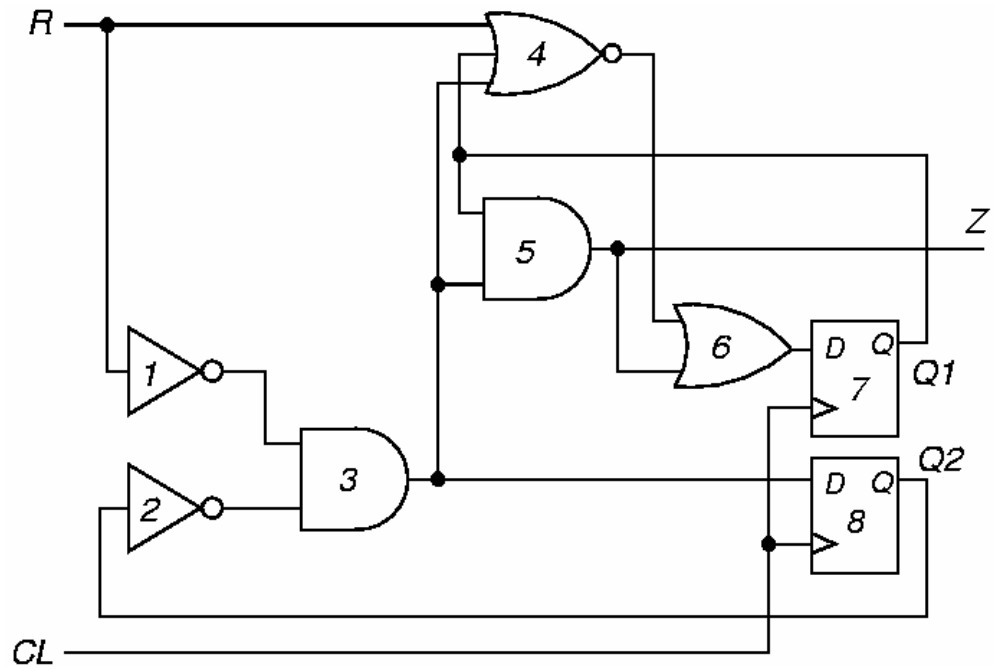
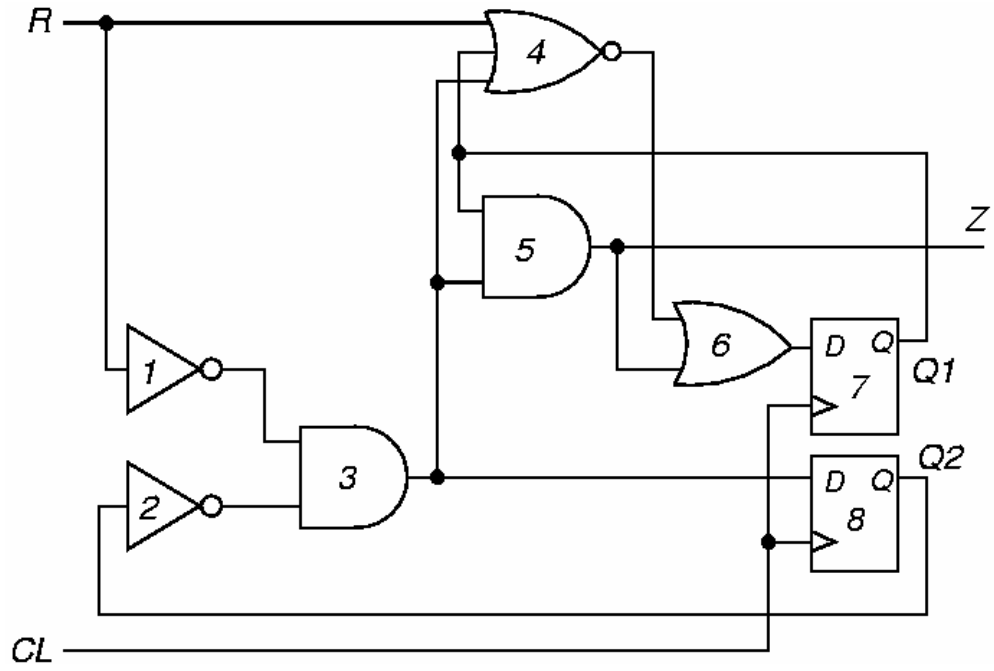


Figure 7. CUT with counter and MISR for Problem 7.

8. (10 pts extra credit). Estimate the total cost of testing a chip using boundary scan. First estimate the cost of the boundary scan hardware for a chip with 256 pins. Transistors cost 24 μ cents/transistor (in 2005). One logic gate uses 4 transistors, one master-slave flip-flop uses 24 transistors, and the IEEE 1149.1 TAP controller uses 262 transistors. Now, given a test vector set of 512,000 vectors for the chip, and a test clock rate of 200 MHz, estimate the cost of testing this chip using IEEE 1149.1 hardware, given that the tester cost is 4.5 cents/s.

Extra sheets for Problem 3.



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