Lecture 26
Logic BIST
Architectures

- Motivation
- Built-in Logic Block Observer (BILBO)
- Test / clock systems
- Test / scan systems
- Circular self-test path (CSTP) BIST
- Circuit initialization
- Loop-back hardware
- Test point insertion
- Summary
Motivation

- Complex systems with multiple chips demand elaborate logic BIST architectures
  - BILBO and test / clock system
    - Shorter test length, more BIST hardware
  - STUMPS & test / scan systems
    - Longer test length, less BIST hardware
  - Circular Self-Test Path
    - Lowest hardware, lower fault coverage
- Benefits: cheaper system test, Cost: more hdwe.
- Must modify fully synthesized circuit for BIST to boost fault coverage
  - Initialization, loop-back, test point hardware
Built-in Logic Block Observer (BILBO)

- Combined functionality of D flip-flop, pattern generator, response compacter, & scan chain
  - Reset all FFs to 0 by scanning in zeros
Example BILBO Usage

- **SI** – Scan In
- **SO** – Scan Out
- Characteristic polynomial: $1 + x + \ldots + x^n$
- **CUTs A and C**: BILBO1 is MISR, BILBO2 is LFSR
- **CUT B**: BILBO1 is LFSR, BILBO2 is MISR

(a) Example test configuration.
BILBO Serial Scan Mode

- B1 B2 = “00”
- Dark lines show enabled data paths
BILBO LFSR Pattern Generator Mode

- B1 B2 = “01”
BILBO in D FF (Normal) Mode

- B1 B2 = "10"
BILBO in MISR Mode

- \( B_1 \ B_2 = \text{"11"} \)
Test / Clock System Example

- New fault set tested every clock period
- Shortest possible pattern length
  - 10 million BIST vectors, 200 MHz test / clock
  - Test Time = \( \frac{10,000,000}{200 \times 10^6} = 0.05 \) s
- Shorter fault simulation time than test / scan
Test / Scan System

- New fault tested during 1 clock vector with a complete scan chain shift
- Significantly more time required per test than test / clock
  - **Advantage:** Judicious combination of scan chains and MISR reduces MISR bit width
  - **Disadvantage:** Much longer test pattern set length, causes fault simulation problems
- Input patterns – time shifted & repeated
  - Become correlated – reduces fault detection effectiveness
  - Use XOR network to phase shift & decorrelate
STUMPS Example

- SR1 ... SRn – 25 full-scan chains, each 200 bits
- 500 chip outputs, need 25 bit MISR (not 5000 bits)
STUMPS

- Test procedure:
  - Scan in patterns from LFSR into all scan chains (200 clocks)
  - Switch to normal functional mode and clock 1 x with system clock
  - Scan out chains into MISR (200 clocks) where test results are compacted
  - Overlap Steps 1 & 3

- Requirements:
  - Every system input is driven by a scan chain
  - Every system output is caught in a scan chain or drives another chip being sampled
Alternative Test / Scan Systems

(a) Simple system.

(b) Alternative system.
BILBO vs. STUMPS vs. ATE

- LSSD: Level-sensitive scan design
- ATE rate: 325 MHz
- System clock rate: 1 GHz
- \( P = \# \text{ patterns} \)
- \( L = \text{max. scan chain length} \)
- \( CP = \text{clock period} = 10^{-9} \text{ s} \)
- \( k = \frac{\text{Self-test speed}}{\text{LSSD tester speed}} = 3.07692 \)

- Test times – BILBO: \( P \times CP \)
- STUMPS: \( P \times L \times CP \)
- ATE: \( P \times L \times CP \times k \)
- External test & ATE: 307 x longer than BILBO
- STUMPS: 100 x longer than BILBO

- Due to extra scan chain shifting
**Circular Self-Test Path (CSTP) BIST**

- Combine pattern generator and response compacter into a single device
- Use synthesized hardware flip-flops configured as a circular shift register
  - Non-linear mathematical BIST system
  - Superposition does not hold
  - Flip-flop self-test cell – XOR’s $D$ with $Q$ state from previous FF in CSTP chain
- MISR characteristic polynomial: $f(x) = x^n + 1$
- Hard to compute fault coverage
CSTP System

Scan_in/Circulate

MUX
0
1

Inputs

Combinational
Logic

Outputs

Internal Flip-Flops

(a) Single scanned flip-flop.
Examples of CSTP Systems

- CSTP BIST for 4 ASICs at Lucent Technologies:
  - Tested everything on 3 of the 4, except for:
    - Input/Output buffers and Input MUX
  - BIST overheads: logic – 20 %, chip area – 13 %
  - Stuck-at fault coverage – 92 %
Circuit Initialization

- Full-scan BIST – shift in scan chain seed before starting BIST
- Partial-scan BIST – critical to initialize all FFs before BIST starts
  - Otherwise we clock X’s into MISR and signature is not unique and not repeatable
- Discover initialization problems by:
  - Modeling all BIST hardware
  - Setting all FFs to X’s
  - Running logic simulation of CUT with BIST hardware
Circuit Initialization (continued)

- If MISR finishes with BIST cycle with X’s in signature, Design-for-Testability initialization hardware must be added

- Add **MS** (master set) or **MR** (master reset) lines on flip-flops and excite them before BIST starts

- Otherwise:
  - Break all cycles of FF’s
  - Apply a partial BIST synchronizing sequence to initialize all FF’s
  - Turn on the MISR to compact the response
Isolation from System Inputs

- Must isolate BIST circuits and CUT from normal system inputs during test:
  - Input MUX
  - Blocking gates –
    - AND gate – apply 0 to 2\textsuperscript{nd} AND input, block normal system input
- Note: Neither all of the Input MUX nor the blocking gate hardware can be tested by BIST
  - Must test externally or with Boundary Scan (covered later)
Loop-Back Circuit

- Loop back outputs into inputs:

- $M = 0$ Normal Operation
- $M = 1$ Loop Back
System Test with Loop-Back

- Exercise entire system with loop-back circuit
- Use Boundary Scan to test chip interconnects
Test Point Insertion

- BIST does not detect all faults:
  - Test patterns not rich enough to test all faults
- Modify circuit after synthesis to improve signal controllability
- Observability addition – Route internal signal to extra FF in MISR or XOR into existing FF in MISR
0 and 1 Injection

- Force $b$ to 0 when $\text{TEST}$ & $S$ are 1
- Force $b$ to 1 when $\text{TEST}$ & $S$ are 1
Test Point Activation

- Four test epochs $\Phi_0, \Phi_1, \Phi_2, \Phi_3$
- Phase decoder: enables different parts at different phases
- Apply specified test pattern count at each
- Example:
  - $g_t = 0$ in $\Phi_1$ & $\Phi_2$, so $c_1 = 0$
  - $g_t = 1$ in $\Phi_0$ & $\Phi_3$, so $c_1 = g$
  - $h_t = 1$ in $\Phi_2$ & $\Phi_3$, so $c_2 = 1$
  - $h_t = 0$ in $\Phi_0$ & $\Phi_1$, so $c_2 = h$
Test Point Activator

Diagram of test point activator with phases and inputs and outputs.
Summary

- Logic BIST system architecture --
  - Advantages:
    - Higher fault coverage
    - At-speed test
    - Less system test, field test & diagnosis cost
  - Disadvantage: Higher hardware cost
- Architectures: BILBO, test / clock, test / scan
- Needs DFT for initialization, loop-back, and test points