Lecture 4
Yield Analysis & Product Quality

- Yield and manufacturing cost
- Clustered defect yield formula
- Yield improvement
- Defect level
- Test data analysis
- Example: SEMATECH chip
- Summary

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A manufacturing defect is a finite chip area with electrically malfunctioning circuitry caused by errors in the fabrication process.

A chip with no manufacturing defect is called a good chip.

Fraction (or percentage) of good chips produced in a manufacturing process is called the yield. Yield is denoted by symbol $Y$.

Cost of a chip:

\[
\text{Cost of fabricating and testing a wafer} \quad \frac{\text{Cost of fabricating and testing a wafer}}{Y \times \text{Number of chip sites on the wafer}}
\]
Clustered VLSI Defects

Unclustered defects
Wafer yield = 12/22 = 0.55

Clustered defects (VLSI)
Wafer yield = 17/22 = 0.77
Yield Parameters

- Defect density \( (d) \) = Average number of defects per unit of chip area
- Chip area \( (A) \)
- Clustering parameter \( (\alpha) \)
- Negative binomial distribution of defects, \( p(x) = \text{Prob (number of defects on a chip = x)} \)

\[
p(x) = \frac{\Gamma(\alpha+x) \cdot (Ad/\alpha)^x}{\Gamma(\alpha) \cdot x! \cdot (1+Ad/\alpha)^{\alpha+x}}
\]

where \( \Gamma \) is the gamma function

\( \alpha = 0 \), \( p(x) \) is a delta function (max. clustering)

\( \alpha = \infty \), \( p(x) \) is Poisson distrib. (no clustering)
Yield Equation

\[ Y = \text{Prob ( zero defect on a chip )} = p \,(0) \]

\[ Y = \left( 1 + \frac{\text{Ad}}{\alpha} \right)^{-\alpha} \]

Example: \( \text{Ad} = 1.0, \alpha = 0.5, Y = 0.58 \)

Unclustered defects: \( \alpha = \infty, Y = e^{-\text{Ad}} \)

Example: \( \text{Ad} = 1.0, \alpha = \infty, Y = 0.37 \)

too pessimistic!
Defect Level or Reject Ratio

- Defect level (DL) is the ratio of faulty chips among the chips that pass tests.
- DL is measured as parts per million (ppm).
- DL is a measure of the effectiveness of tests.
- DL is a quantitative measure of the manufactured product quality. For commercial VLSI chips a DL greater than 500 ppm is considered unacceptable.
Determination of DL

- From field return data: Chips failing in the field are returned to the manufacturer. The number of returned chips normalized to one million chips shipped is the DL.

- From test data: Fault coverage of tests and chip fallout rate are analyzed. A modified yield model is fitted to the fallout data to estimate the DL.
Modified Yield Equation

- Three parameters:
  - Fault density, \( f = \) average number of stuck-at faults per unit chip area
  - Fault clustering parameter, \( \beta \)
  - Stuck-at fault coverage, \( T \)

- The modified yield equation:
  \[
  Y(T) = \left(1 + TAf / \beta\right)^{-\beta}
  \]

Assuming that tests with 100% fault coverage (\( T = 1.0 \)) remove all faulty chips,

\[
Y = Y(1) = \left(1 + Af / \beta\right)^{-\beta}
\]
Defect Level

\[
DL(T) = \frac{Y(T) - Y(1)}{Y(T)}
\]

\[
= 1 - \left( \frac{\beta + T Af}{\beta + Af} \right) \beta
\]

Where \( T \) is the fault coverage of tests, \( Af \) is the average number of faults on the chip of area \( A \), \( \beta \) is the fault clustering parameter. \( Af \) and \( \beta \) are determined by test data analysis.
Example: SEMATECH Chip

- Bus interface controller ASIC fabricated and tested at IBM, Burlington, Vermont
- 116,000 equivalent (2-input NAND) gates
- 304-pin package, 249 I/O
- Clock: 40MHz, some parts 50MHz
- 0.45\(\mu\) CMOS, 3.3V, 9.4mm x 8.8mm area
- Full scan, 99.79% fault coverage
- Advantest 3381 ATE, 18,466 chips tested at 2.5MHz test clock
- Data obtained courtesy of Phil Nigh (IBM)
Test Coverage from Fault Simulator

![Graph showing stuck-at fault coverage vs vector number](image)
Measured Chip Fallout
Model Fitting

![Graph showing chip fallout and computed 1-Y(T)]

- Measured chip fallout: $Y(1) = 0.7623$
- $Y(T)$ for $Af = 2.1$ and $\beta = 0.083$
Computed DL

237,700 ppm (Y = 76.23%)
Summary

- VLSI yield depends on two process parameters, defect density \( (d) \) and clustering parameter \( (\alpha) \)
- Yield drops as chip area increases; low yield means high cost
- Fault coverage measures the test quality
- Defect level \( (DL) \) or reject ratio is a measure of chip quality
- \( DL \) can be determined by an analysis of test data
- For high quality: \( DL < 500 \text{ ppm} \), fault coverage \( \sim 99\% \)
Yield References

  - contains exhaustive survey of all yield modeling research from the beginning in 1960 to 1987.