

CPSC 489-501  
Hardware-Software Codesign of Embedded System  
Test 1

**Maximum Points 100**

**Maximum duration 50 Mins**

*(Answers must be brief and to the point, give best answer among possible choice of answers, provide assumptions in case you adopt one)*

1. Comment on the use of IP cores in embedded system codesign. (5 points)
  - *Cores are standardized for reuse as system building blocks*  
*Rationale: leveraging the existing software layers including OS and applications in embedded system. This results to customized VLSI chip with better area/ performance/ power trade-off and Systems on Silicon.*
2. Which of the following statement is true for embedded system's programming? (5 points)
  - (a)
  - (b) *Most software is already provided by system integrator who could be application developer too.*
  - (c)
3. Fill the blanks. (application specific compilers, hardware utilization, sequences to sequences) 6 points
  - (a) Goal of codesign in ISP development is to optimize hardware utilization by application and operating system.
  - (b) In case of ASIPs, the price of the flexibility in choosing mixed instruction set is to develop the application specific compilers.
  - (c) In dataflow model of computation, we consider the actors mathematically as functions from sequence to sequence.
  - (d) The goal of extended partitioning is to combine implementation bins with binary partitioning.
4. Draw the codesign framework using a flow diagram. Indicate the activities of each block in the flowchart. (10 points)

*Standard flow-chart from the lecture note.*
5. Why does the software synthesis in embedded system is more constrained compared to general computing system design? (6 points)
  - *swapping devices, no stacks, and only polling and static variables*

6. What are the features of a good computational model? (5 points)

- *formal* : no ambiguity
- *complete* : with sets of properties, performance indices and constraints
- *comprehensive* and easy to modify
- *natural* to understand

7. Why the interface verification is important? (6 points)

- *Interface verification separates design to distinct components. The components interact through interface using coordination mechanism following some protocol.*
    - *Designers might treat details on signaling differently across various components. Leads to inconsistency.*
- ⇒ *Interface verification checks this inconsistencies.*

8. Describe the bounded FIFO buffer as communication primitive in TSM context. (6 points)

- *Each input and output signals are internally totally ordered. For buffer size = 1, input and output events must interleaved. For larger size, impose the maximum difference between input or output events occurring in succession.*

9. Draw the FSM of mod3 counter. Present an Estrel version to your counter. What are the disadvantages of FSM? (12 points)

*Guess your self starting from simple FSM with three states.*

10. Given the following DF network, balance for each edge. (6 points)

*See the lecture note*

11. Draw the CFSM network of seatbelt example discussed in the class. Give the formal descriptions of input and triggering events. (10 points)

- *Refer slide 22 of CFSM lecture.*

12. What is cost function in partitioning? Can you state the cost function model that considers bus and processor utilization? (8 points)

- *From a given set of sequencing graph models and timing constraints, create two sets of sequencing graph models such that one can be implemented in hw and the other in sw and the following is true:*
  - *timing constraints are satisfied for the two sets of graph models*
  - *processor utilization,  $P \leq 1$*
  - *bus utilization,  $B \leq B'$*
  - *A partition cost function,  $f = f(S_H, B, P^{-1}, m)$  is minimized.*

13. What is the goal of pre-clustering in three phase functional partitioning? How is it different from other two steps? (8 points)

- *Goal: Reduce the number of procedures for subsequent N-way assignment by merging procedures whose separation among parts would never represent good solution.*
- *Different from granularity step: procedures being clustered here may not be such that they could be merged into single new procedure. I.e. calls to these procedure are non-adjacent.*
- *Different from N-way assignment: each cluster does not represent a processor and therefore can not be guided by direct design metrics estimates.*

14. Draw the GCLP flow graph and label the role in each node. (7 points)  
*Slide 11 in partition III.*