Assignment 2: Virtual Prototyping – Creating & Incorporating Models into SoC Designer using Modelstudio

This assignment will give you experience on how to create a "carbon model" from RTL, incorporate it into a SoC design and analyze its impact on your design. This tutorial uses the A9 MP1 AXI system from the previous tutorial.

This assignment will focus on the use of Carbon Model Studio. You will create an Interrupt Controller's carbon model from RTL using ModelStudio. You will use this newly created Interrupt Controller model to replace the pre-existing one in the A9 Reference design (i.e. VIC_PL190). You will then run the sample sort application using this reconfigured system as in Assignment 3 and examine its behavior.

A reference Interrupt Controller is provided in: /opt/cpak/Interrupt.v

The procedure for accessing the Carbon tools remains the same as in Assignment 3. The tutorials are in: /opt/carbon_tutorials/

1. Using-Socd-basic-workbook.pdf
2. Platform-integration-SoCD-workbook.pdf
3. CoSimulation-workbook.pdf

You will be focusing on Platform Integration SoC Designer in this assignment.

What to Turn in:

Execute the steps in the tutorial – "Platform Integration SoC Designer Workbook" (Platform-integration-SoCD-workbook.pdf).

1. Answer the following questions with respect to the tutorial: (3 points)
    a. What are the names and locations of the shared objects for the Interrupt model you created? (They will be in your project folder) (1 point)
    b. Show a screenshot of the profiling window (with respect to stream0), register window for the system when (1) the first break point is hit at Cycle 0? (1 point)
    c. When does your simulation end, what is your estimate about the performance of the reference interrupt controller? Is it an efficient design? (1 point)
2. Replace the provided CM_timer_Apb module in the A9 MP1 AXI reference design with your own module using the same process as shown in the tutorial. (7 points)
    a. You will need to first understand the AM_timer_Apb module's functionality. Refer to

/opt/Release_Amba/CM_Timer_Apb/Default/CML_APB_Timer_User.pdf to understand what this module does. (1 point)

b. You will need to write RTL code for the replacement module, validate its functionality using ModelSim. You may also need to refer to Ref. [5] to better understand the specifications. (2 points)
c. Generate a Carbon Model from your RTL. Clearly describe the ESL transactor ports you are mapping to generate the model. (2 points)
d. Incorporate your model into the A9 Reference Design, simulate the system and report the resulting execution time with screenshots. (2 points)
e. BONUS: Define and include debug registers, profiling streams for your replacement module as you did in the tutorial (Pages 17-21) for the interrupt controller. This will help you master this process. (2 points)

3. BONUS Question: Validate the behavior of the reference Interrupt controller RTL (/opt/cpak/Interrupt.v) using ModelSim. (3 points)

References:

1. Application Notes and User guides in $MAXSIM_HOME/doc on cse-codesign.tamu.edu
2. User Guides in /opt/documents on cse-codesign.tamu.edu
3. ARM Generic Interrupt Controller Architecture: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ihi0048a/index.html
4. Carbon APB Timer Model User Guide in /opt/Release_Amba/CM_Timer_Apb/Default/CML_APB_Timer_User.pdf on cse-codesign.tamu.edu
5. ARM Dual Timer Module – ARM Technical Reference Manual – http://infocenter.arm.com/help/topic/com.arm.doc.ddi0243c/I1017633.html
6. ARM – Example APB Slave - http://infocenter.arm.com/help/topic/com.arm.doc.ddi0243c/I1030490.html

Notes “Platform Integration SoC Designer Workbook” (Platform-integration-SoCD-workbook.pdf):

(1) The cycle counter on the toolbar when the system requests input appears to be 16752 (Page 38).
(2) When setting up paths in the component library for $MAXSIM_PROTOCOL/etc/Protocols.conf, you may have to type in : ${MAXSIM_HOME}/etc/Protocols.conf. Note that it points to /opt/SoCDesigner/Protocols/etc/Protocols/conf (Page 28)
(3) The second component configuration you may need to add is: ${MAXSIM_HOME}/CDP/Linux/4.1.0/Cosimulation/transactors/etc/Cosim_Transactors.conf (Page 28)

(4) ModelSim-SE 10.1 d is also installed on cse-codesign.tamu.edu. You can access it from the command line using: vsim
(5) A ModelSim tutorial is available in: /opt/ModelSim-SE-10.1d/modeltech/docs/pdfdocs/ modelsim_se_tut.pdf

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