Assignment 3: Cosimulation – Using a Virtual prototyping tool (Carbon SoC Designer) with an external RTL Simulator

This assignment will give you experience of how to use Carbon SoC Designer to simulate with an external RTL simulator. In class, we discussed Cosimulation as a "technique to simulate individual components using different best-in-class simulation tools that exchange information in a collaborative manner".

In this lab, you will be using Mentor's ModelSim for HDL simulation (see signal waveforms) and Carbon's SoCDesigner for architectural profiling simultaneously. This tutorial uses the A9 MP1 AXI system as in the previous assignments.

In this assignment, you will delete the Vic_Pl190 Interrupt controller component (from the reference design); add a special transactor component, which enables exporting of the AHB signals (for the Vic_Pl190) out of the SoCDesigner simulation kernel into the ModelSim simulation kernel. The ModelSim simulation in turn will consist of two modules bound together by a top-level test bench – the first module exposes the exported signals, the second contains the Interrupt Controller's RTL (Interrupt.v as in Assignment 4).

You will make the CLK and Reset signals traverse ModelSim into the SoCDesigner kernel; the AHB, timerInterrupt, Core InterruptRequest signals traverse SoCDesigner into ModelSim; and use the combined tool chain to run the "Cosimulation".

You will run the sample sort application using this co-simulated system as with the previous assignments. Note that the CLK and reset signals are part of the RTL testbench and manage the synchronization (master-slave Cosimulation). You shall be able to identify the benefits of co-simulation at the end of this assignment:

1. Early access to hardware design for software engineers
2. "Realistic" stimulus (AHB bus signals) for hardware simulation (Interrupt controller) available as compared to "unrealistic" testbench waveforms.
3. Better control and visibility into the SoC design for both SW & hardware programmers.

The reference Interrupt Controller is provided in: /opt/cpak/Interrupt.v
The reference Test Bench is provided in : /opt/cpak/tb.v
The reference Makefile is provided in: /opt/cpak/Makefile

The procedure for accessing the Carbon tools remains the same as in Assignment 3,4. The tutorials are in: /opt/carbon_tutorials/. We will focus on #3.
1. Using-Socd-basic-workbook.pdf
2. Platform-integration-SoCD-workbook.pdf
3. CoSimulation-workbook.pdf

Part (b) of this assignment will be posted later this week.

What to Turn in for Part (a):

Execute the steps in the tutorial – "Cosimulation Workbook" (CoSimulation-workbook.pdf).

1. Answer the following questions with respect to the tutorial: (6 points)
    a. Show a screenshot of the final system you build on SoC Designer canvas after enabling the CoSimulation feature with Modelsim (1 point)
    b. Show a screenshot of the Modelsim Waveform window with the exported signals from the tb/mx instance at approximately 533200 ns? (1 point)
    c. Comment on/discuss the changes that you observe on the AHBV2 bus signals at this time? You could consult the documents in the references to get an understanding of AHBv2 (in particular Sec. 3.1 – 3.5 of [1]). The source code for the sort example application is also included in /opt/cpak/A9-MP-AXI-Demo-CMS5.14.0-V2012.11.09-SOCD7.11.0/Applications/sort/ for your reference. (4 points)
2. BONUS: AHBV2s_T2S component is used in the tutorial to export the AHB version2 slave transactor to their corresponding signals. The test bench integrates the exported signals and the provided Interrupt.v code into a top-level module for co-simulation. Likewise, the APB_T2S component enables the export/conversion of the AMBA APB transactor to their corresponding signals. Replace the CM_Timer_APB component in the A9 reference design with this module, select the APB signals to be exported in the HDL Cosimulation setup, write a new top-level test-bench to integrate maxsim and your timer module (from the previous assignment). This will enable you to verify the timer module replacement with real APB bus signals. Include screenshots with description of all steps you undertake to achieve this in your submission. (6 points)

References:

1. AMBA AHB Specification in AMBA Specification: (Rev. 2.0) Chapter 3 (Pages 3-1 to 3-54): /opt/documents/arm_specs/AMBA_SPEC.pdf
2. Carbon AHB Transactor User Manual : /opt/carbon/userdoc/pdf/ahb-guide.pdf
3. SoC Designer AHBv2 Protocol Bundle User Guide: /opt/SoCDesigner/doc/AHBv2_Protocol_Bundle_UG.pdf
4. To learn more about Cosimulation, Carbon SoC Designer HDL Cosimulation Guide : /opt/SoCDesigner/doc/SoCDesigner_CDP_HDL_CoSim_Guide.pdf

Notes "Cosimulation Workbook" (CoSimulation-workbook.pdf):

(1) (Page 4) The CPAK Installation directory is /opt/cpak. You will be using the A9-MP1-Training system in /opt/cpak/A9-MP-AXI-Demo-CMS5.14.0-V2012.11.09-SOCD7.11.0/Systems/A9-MP1-TRAINING/. Please copy it into your home directory.
(2) (Page 8) The AMBA Install area on the provided platform is /opt/Release_Amba/gcc.conf
(3) (Page 17) Please make sure that the PinNames, Bitwidth are exactly the same as in Fig. 16; the provided testbench (tb.v) instantiates the module maxsim (in maxsim.v) with those exact portnames & widths.
(4) A ModelSim tutorial is available in: /opt/ModelSim-SE-10.1d/modeltech/docs/pdfdocs/ modelsim_se_tut.pdf

Contact: (d.dharanidhar@tamu.edu) for tool access related problems.