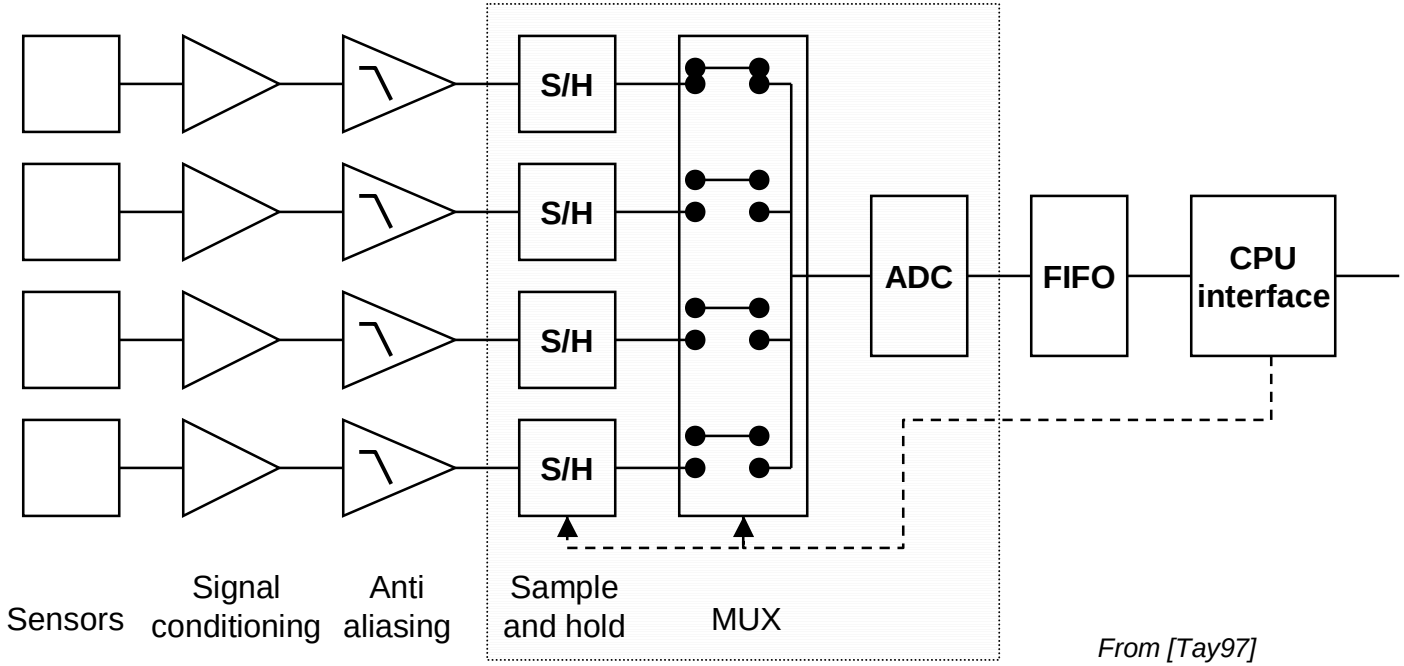
Lecture 8: Data Acquisition II

- Sample and hold
- Multiplexing
- Analog to digital conversion
- Digital to analog conversion

Architecture of data acquisition systems



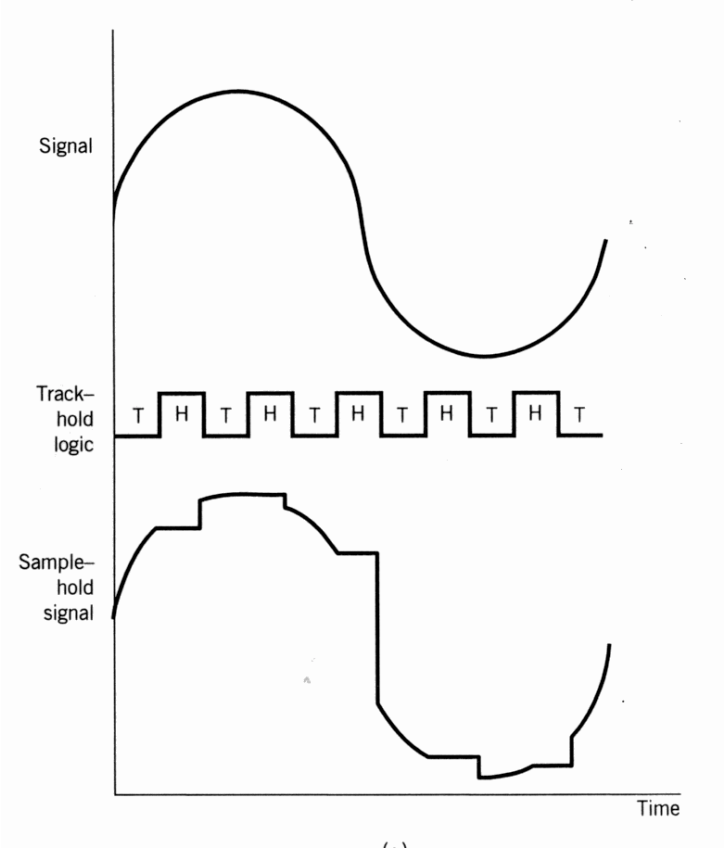
From [Tay97]

Lecture 8

Sample and hold

- **A Sample and hold (S/H) circuit has two basic operating modes**
  - **Sample mode**: The output follows the input
  - **Hold mode**: The output is held constant until sample mode is resumed

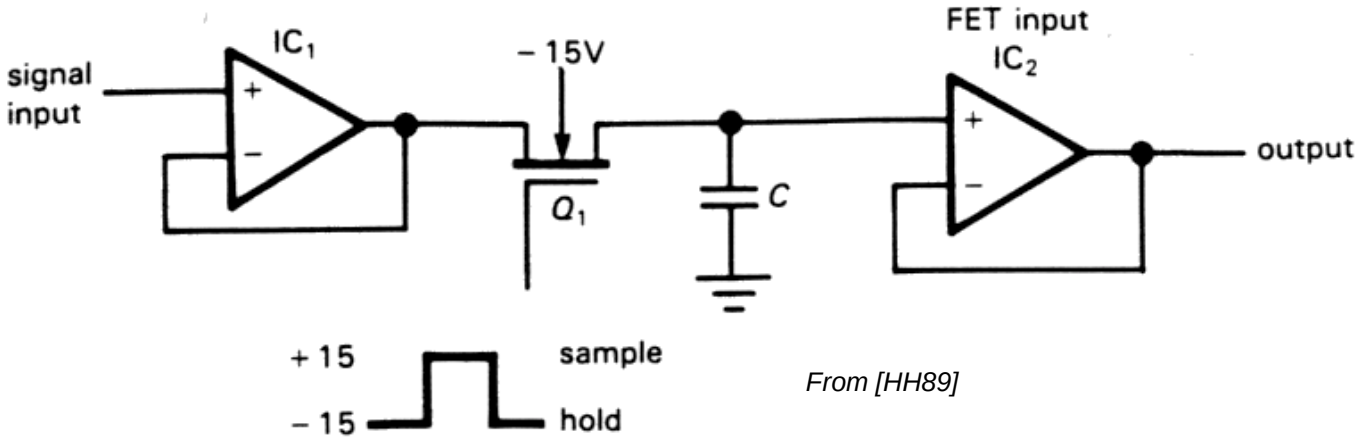
- **The main application of S/H circuits is to hold the input signal to an ADC constant during conversion**
  - Why? Imagine trying to photograph a moving object!



From [FB00]

Basic S/H circuit

- **Basic elements**
  - Voltage followers
  - FET switch

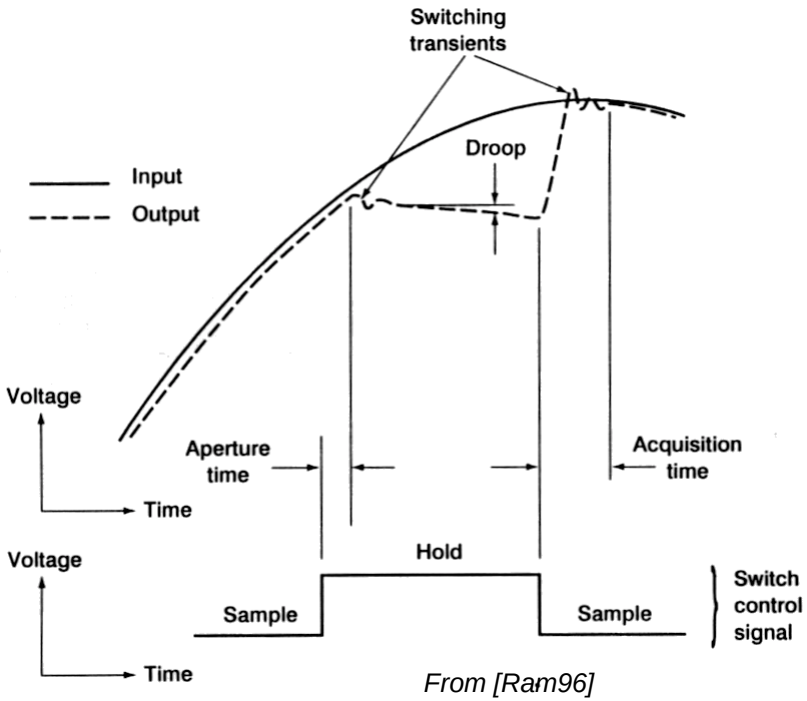


From [HH89]

- **Operation**
  - IC1 provides low Z_{out} version of input signal
  - Q1 passes the signal during ‘sample’ and disconnects during ‘hold’
  - C preserves the value during ‘hold’
  - IC2 is a high Z_{in} op-amp to minimize capacitor discharge during ‘hold’

S/H response characteristics

- **Response parameters**
  - Aperture time: time required for the switch to open (~50ns)
  - Droop: capacitor discharge
  - (~1mV/ms)
  - Acquisition time: switch operation plus capacitor charging time

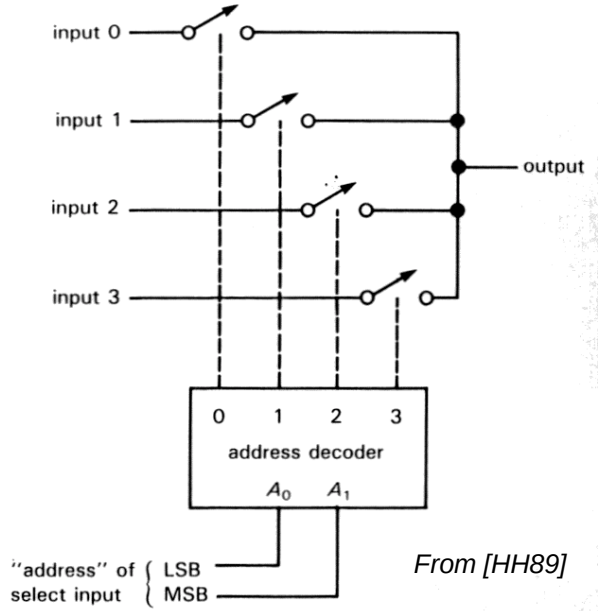


From [Ram96]

- **Considerations for choosing C**
  - C should be large enough to minimize 'droop' caused by leakage currents in Q1 and IC2
  - C should be small enough to track fast signals since it forms a low-pass filter with Q1's ON resistance!
    - In practice, the slew rate of the entire circuit is determined by IC1's output current and Q1's ON resistance

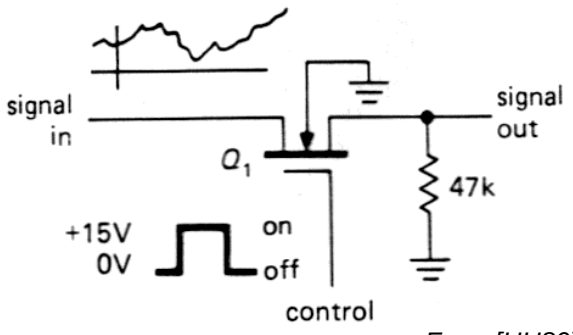
Multiplexers

- **A multiplexer is a circuit that allows you to select any of several inputs, as specified by digital control signals**
  - Since analog switches are bi-directional, this circuit could also be used as a de-multiplexer!
    - It could also be uses as a digital MUX since logic levels are just voltages



From [HH89]

- **FET analog switches**
  - N-channel enhancement-mode MOS-FET
    - When Gate is grounded or negative, the FET is non-conducting
      - Drain-source resistance in the order of 10,000MΩ
    - Bringing the Gate to +15V puts the drain-source channel into conduction
      - Drain-source resistance in the order of 100Ω



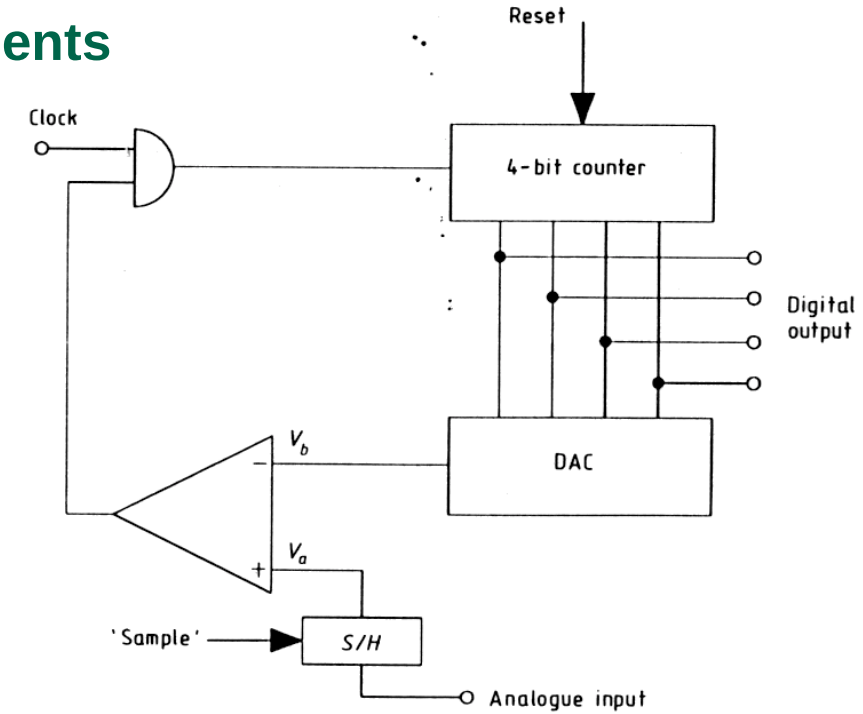
From [HH89]

Analog-to-digital converters

- Single slope or ramp
- Successive approximation
- Dual slope
- Parallel or ‘flash’

Single slope or ramp ADC

- **Composed of three basic elements**
  - A binary counter
  - A digital-to-analog converter
  - An analog comparator

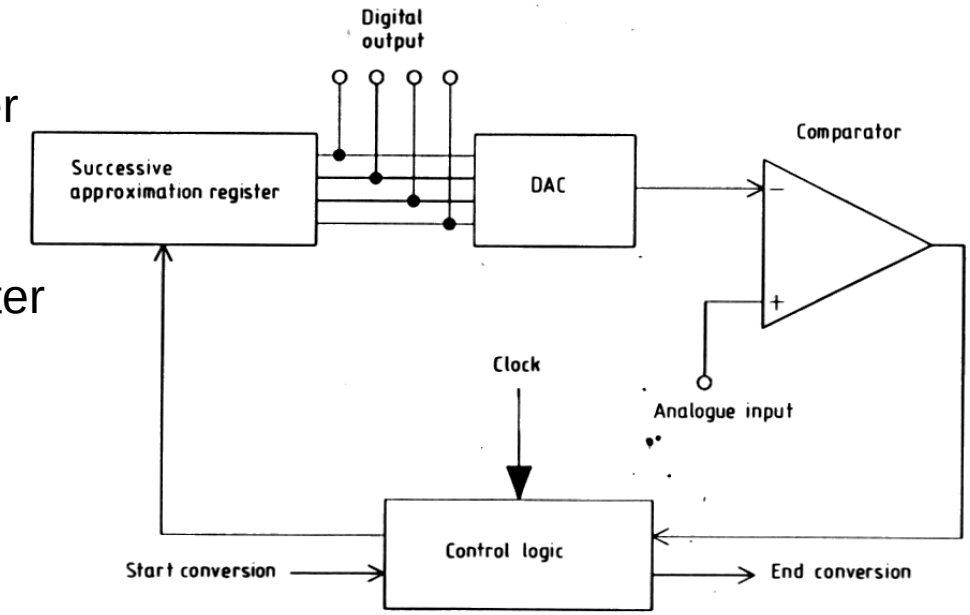


From [BW96]

- **Operation**
  - Counter is reset
  - Analog input is sampled
  - While $V_A > V_B$ counter increments
  - When $V_A = V_B$ counter stops and binary code is available at the output
- **Characteristics**
  - Relatively slow since conversion time could be up to 2^N, where N is the resolution of the ADC

Successive approximation ADC

- **Basic elements**
  - A digital-to-analog converter
  - An analog comparator
  - A control logic module
  - A successive approx. register



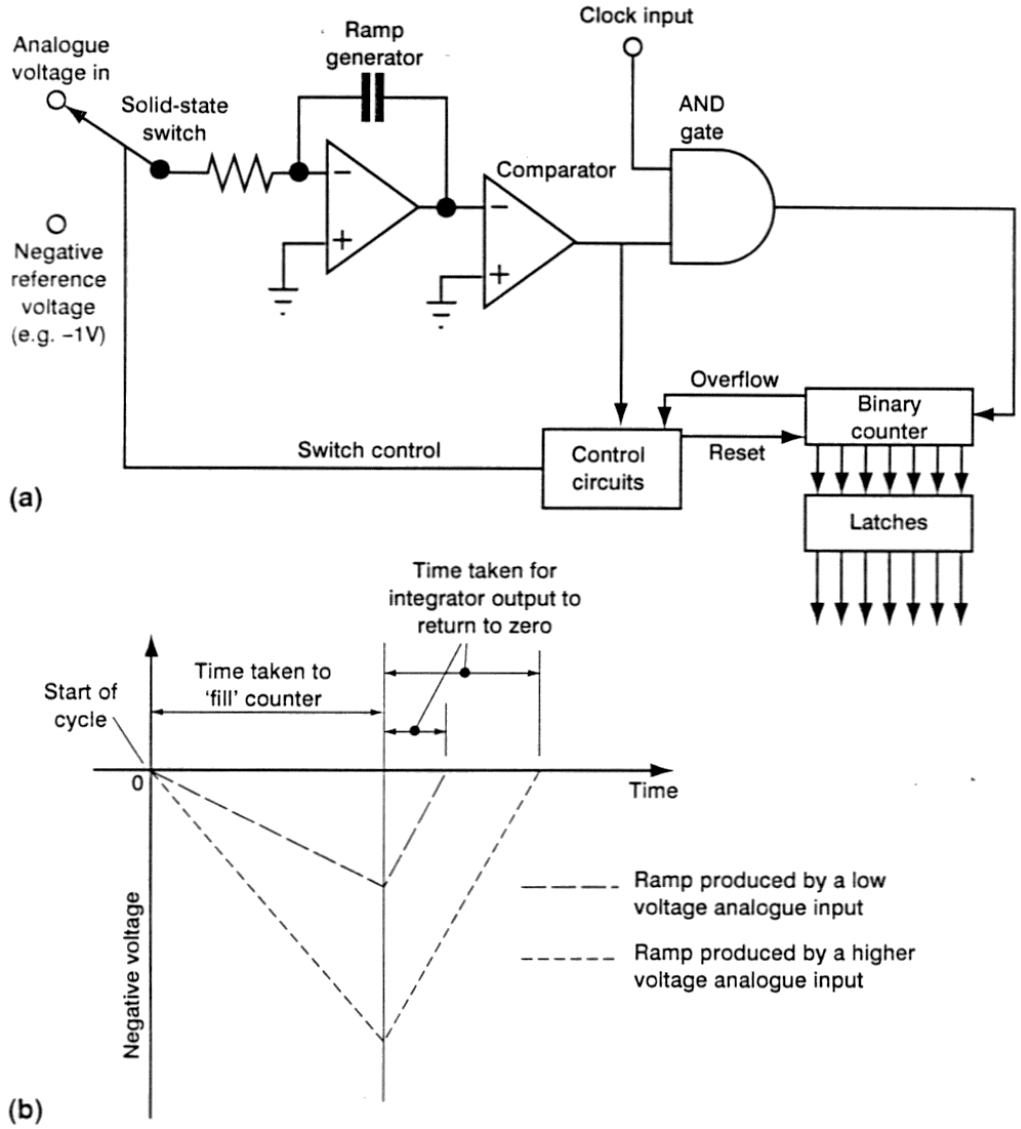
From [BW96]

- **Operation is based on a binary search**
  - Initially, the register provides an output corresponding to half the range (1000…0)
    - If the analog input is greater, then MSB=1, else MSB=0
  - The register performs the same operation from MSB to LSB
- **Characteristics**
  - Conversion requires only N steps, where N is the resolution of the ADC
    - Conversion times of μs are typical

Dual slope ADC

- **Basic elements**
  - An integrator
  - A zero-crossing detector
  - A binary counter
  - Logic gates and switches
- **Operation**
  - Counter is reset and switch is connected to the analog input
    - The integrator generates a negative ramp whose slope is proportional to the analog input
    - The comparator goes HIGH, enabling clock pulses into the counter
  - When counter overflows, it resets to zero and the control circuit switches the switch to a reference negative voltage
    - This causes the integrator to generate a positive slope ramp
    - When this ramp reaches zero, the comparator goes low and stops the counter, whose value represents the analog input
- **Characteristics**
  - Very high resolution, but also slower (30 conversions/sec)
    - Widely used in digital multi-meters
  - Insensitive to clock drift, RC drifts and high-frequency noise

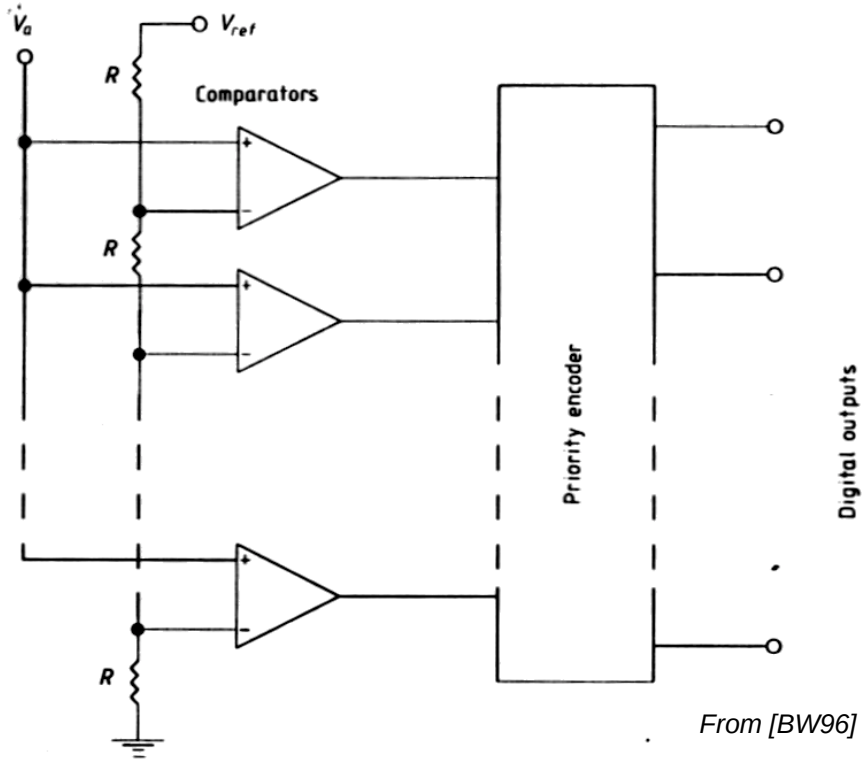
Dual slope ADC



From [Ram96]

Parallel or flash ADC

- **Basic elements**
  - A multiple voltage divider
  - A set of comparators
  - A priority encoder



From [BW96]

- **Operation**
  - Analog input applied to all comparators
  - Priority encoder converts comparator pattern into binary
    - E.g.: A 3-bit ADC:
      - For comparator outputs of 0001111, priority encoder generates 100
      - For comparator outputs of 0111111, priority encoder generates 110

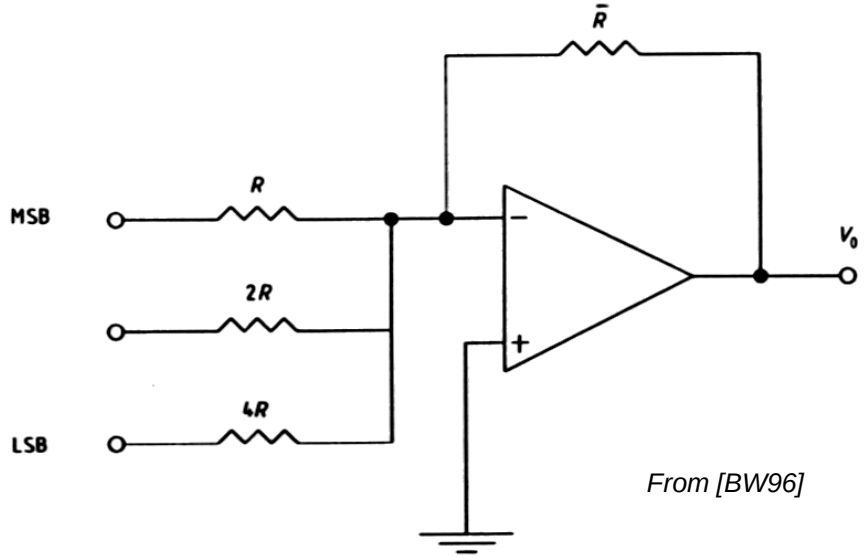
- **Characteristics**
  - Very fast (e.g., 8-bit ADCs capable of 20 million conversions/sec)
  - Very expensive for large N since the number of comparators is 2^N-1

Digital-to-analog converters

- Binary weighted ladder
- R-2R ladder
- Pulse width modulation

Binary weighted ladder

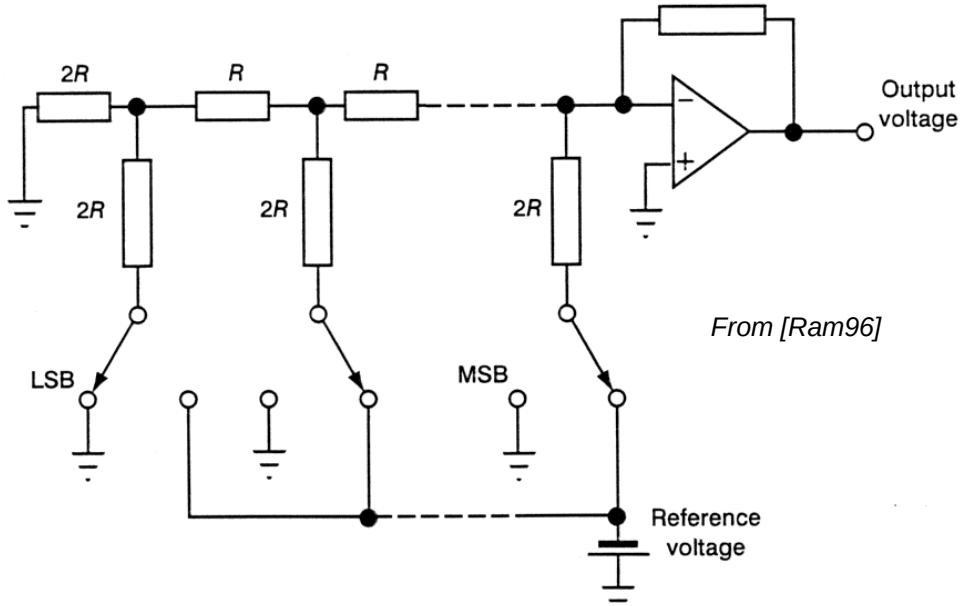
- **Based on the summing op-amp circuit from lecture 5**
  - Each input resistor is twice the value of the previous one
  - Inputs are weighted according to their resistors
- **Characteristics**
  - The lowest value resistor R affects the MSB and must have the highest precision
  - This circuit is impractical for large N since it would require high precision resistors for a wide range



From [BW96]

R-2R ladder

- **Basic elements**
  - 2N resistors
  - An op-amp
  - N switches

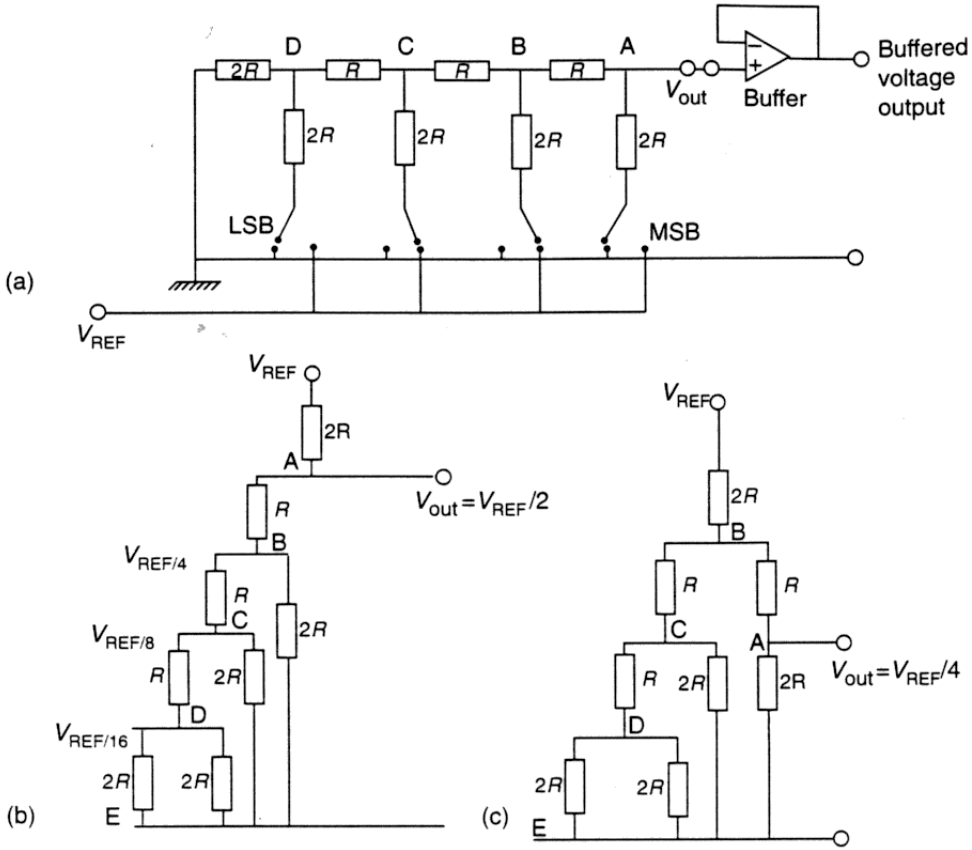


From [Ram96]

- **Operation**
  - Switches
    - When bit I_k=1, the corresponding switch is connected to V_{REF}
    - When bit I_k=0, the corresponding switch is connected to GND
  - Assume all the legs but one are grounded
    - The one connected to V_{REF} will generate a current that flows towards the inverting input of the op-amp
    - This current is halved by the resistor network at each node
    - Therefore, the current contribution of each input is weighted by its position in the binary number

R-2R ladder

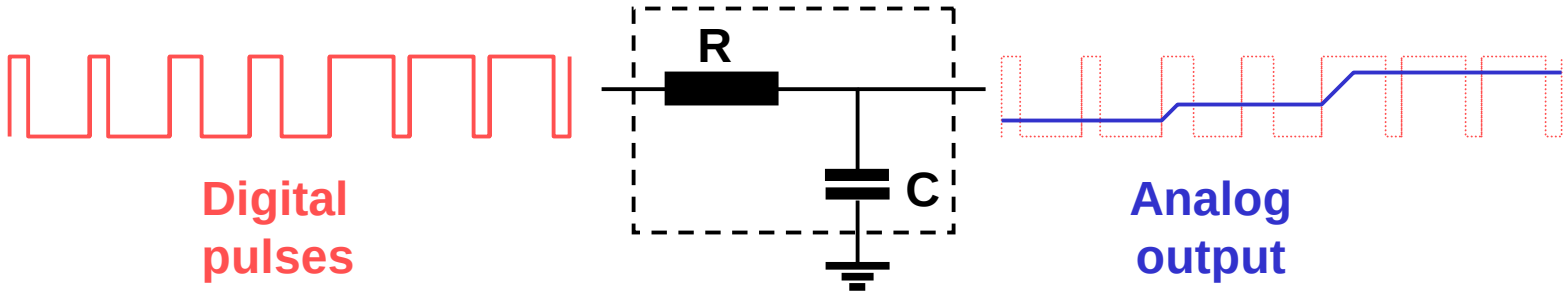
- **The R-2R operation is better understood by redrawing the resistor network**
  - In (b) only the MSB is ON
  - In (c) only the next bit to the MSB is ON



From [Tay97]

Pulse Width Modulation

- **Basic components**
  - A digital line
  - An RC low-pass filter
- **Operation**
  - The digital line is used to generate a train of pulses of fixed frequency
  - The width (duty cycle) of the pulse is made proportional to the desired analog output
  - The pulse train is then passed through a low-pass filter, which generates an output voltage proportional to the average time spent in the HIGH state



References

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[BW96] J. Brignell and N. White, 1996, Intelligent Sensor Systems, 2nd Ed., IOP, Bristol, UK.

[FB00] R. S. Figliola and D.E. Beasley, Theory and design of Mechanical Measurements, 3rd Ed., Wiley, New York.